



UMLEmb:

UML for Embedded Systems

III. System Validation

Ludovic Apvrille,
ludovic.apvrille@telecom-paris.fr

LabSoC, Sophia-Antipolis, France



Goals

Learning objective

- Checking a SysML/AVATAR model against logical errors
 - Checking a SysML/AVATAR model against temporal errors

Content

- Simulation
 - Formal verification
 - Safety properties, observers
 - Prototyping

Model Simulation



Formal verification



Rapid prototyping and code generation



Outline

Model Simulation

Introduction

Formal verification

Rapid prototyping and code generation

Simulation

Simulation enables model debugging and therefore the early detection of design errors in the life cycle of the system

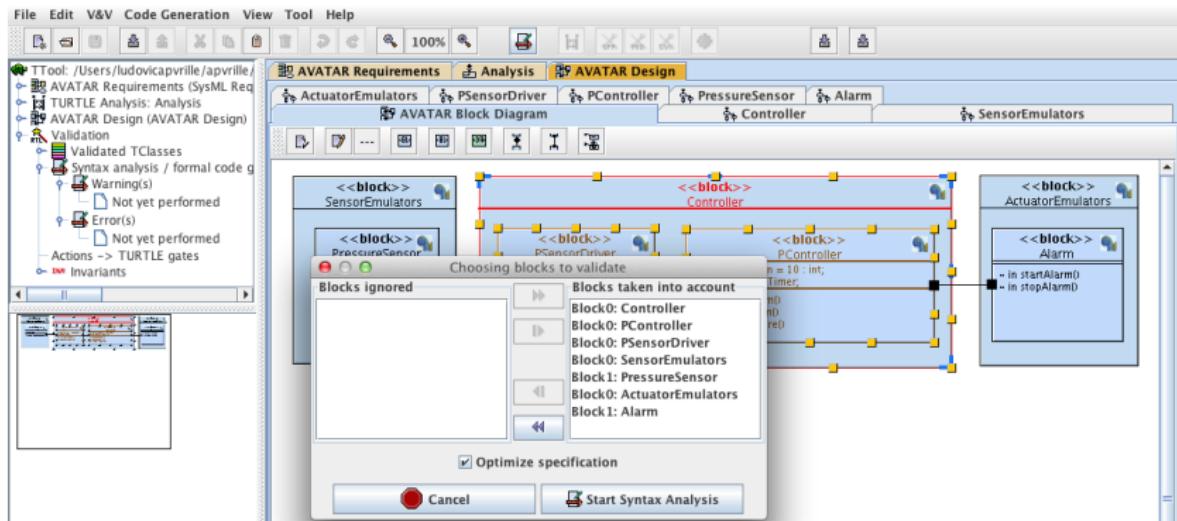
Driving the simulation

- Step by step simulation
 - "Random" simulation
 - Breakpoints

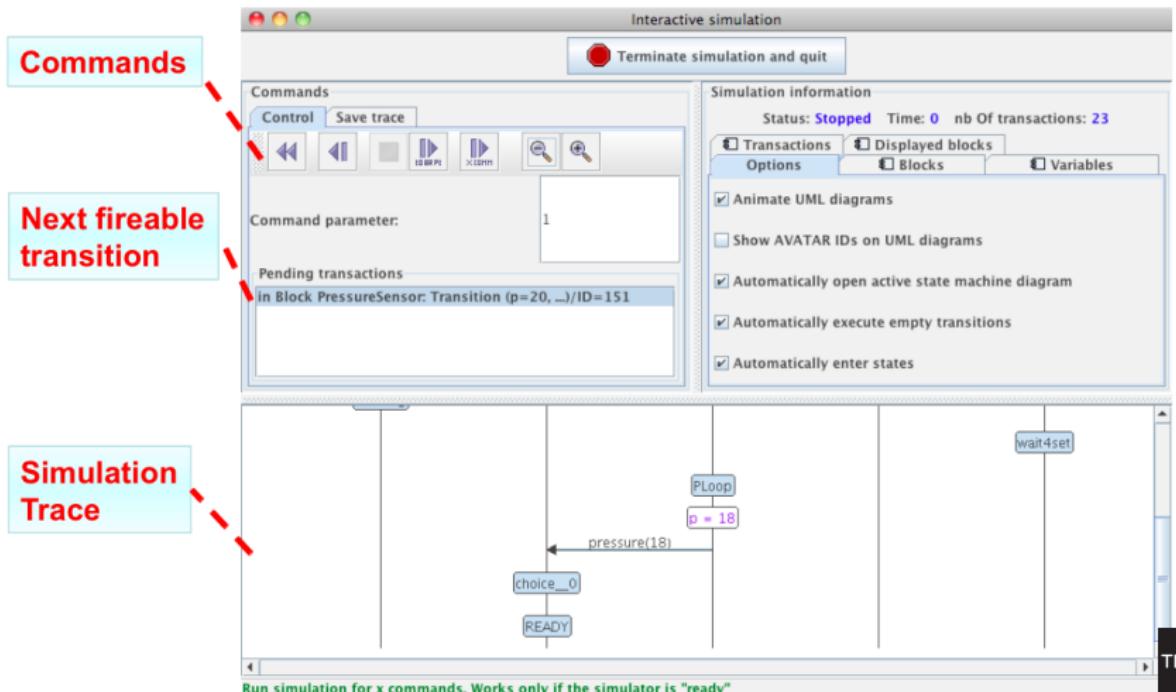
Tracing the simulation

- Simulation trace in the form of a sequence diagram
 - Each already visited branch within each state machine is clearly identified
 - Attribute values may be displayed

Checking Design Diagrams against Syntax Errors



Simulator Interface

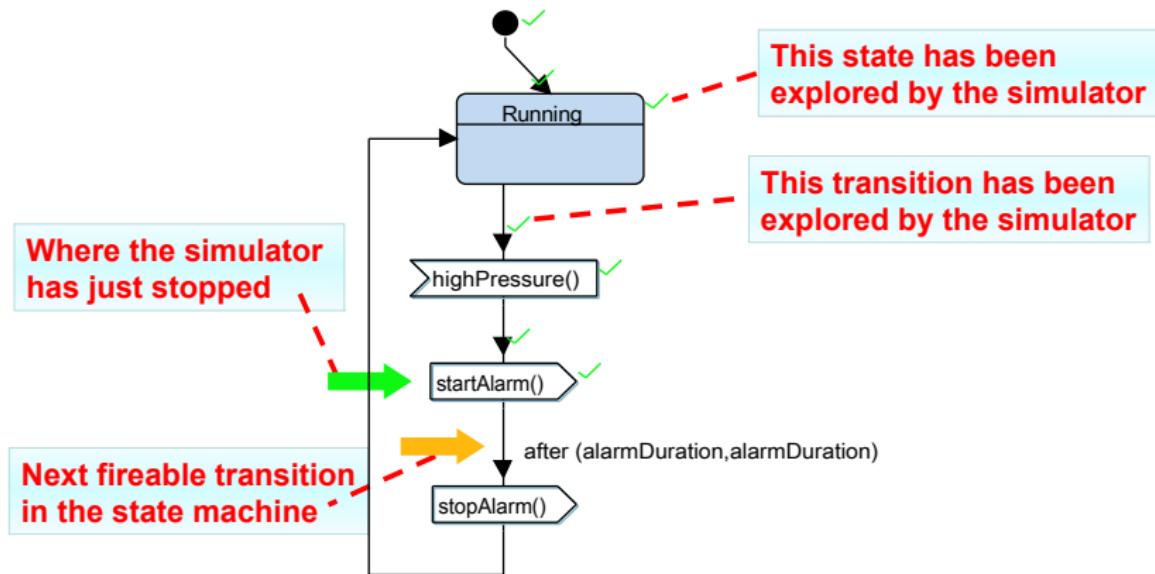


Simulator Trace (Sequence Diagram)

The diagram illustrates a statechart sequence with the following states and events:

- Initial State:** A state labeled `p = 20`.
- Transition 1:** Triggered by `pressure(20)`, leading to a state labeled `choice_0`.
- Transition 2:** Triggered by `highPressure()`, leading to a state labeled `READY`.
- Transition 3:** Triggered by `startAlarm()`, leading to a state labeled `WaitForStop`.
- Transition 4:** Triggered by `@10`, leading to a state labeled `10`.
- Transition 5:** Triggered by `stopAlarm()`, leading to a state labeled `Running`.
- Final State:** A state labeled `waitingForStart`.

Simulator Trace within a State Machine



Outline

Model Simulation

Formal verification

Introduction

Global view in TTool

Properties

Observers

Introduction to Formal Verification

Formal verification intends to explore all possible system execution paths, and to verify properties along those execution paths

Content

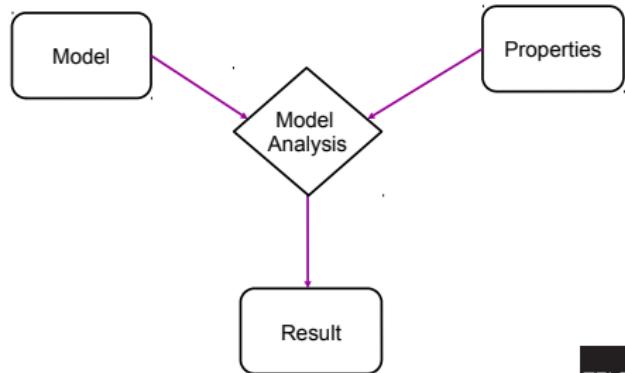
- Brief introduction on formal verification
 - How to model and prove safety properties
 - Example: the pressure controller

Simulation vs. Formal Verification

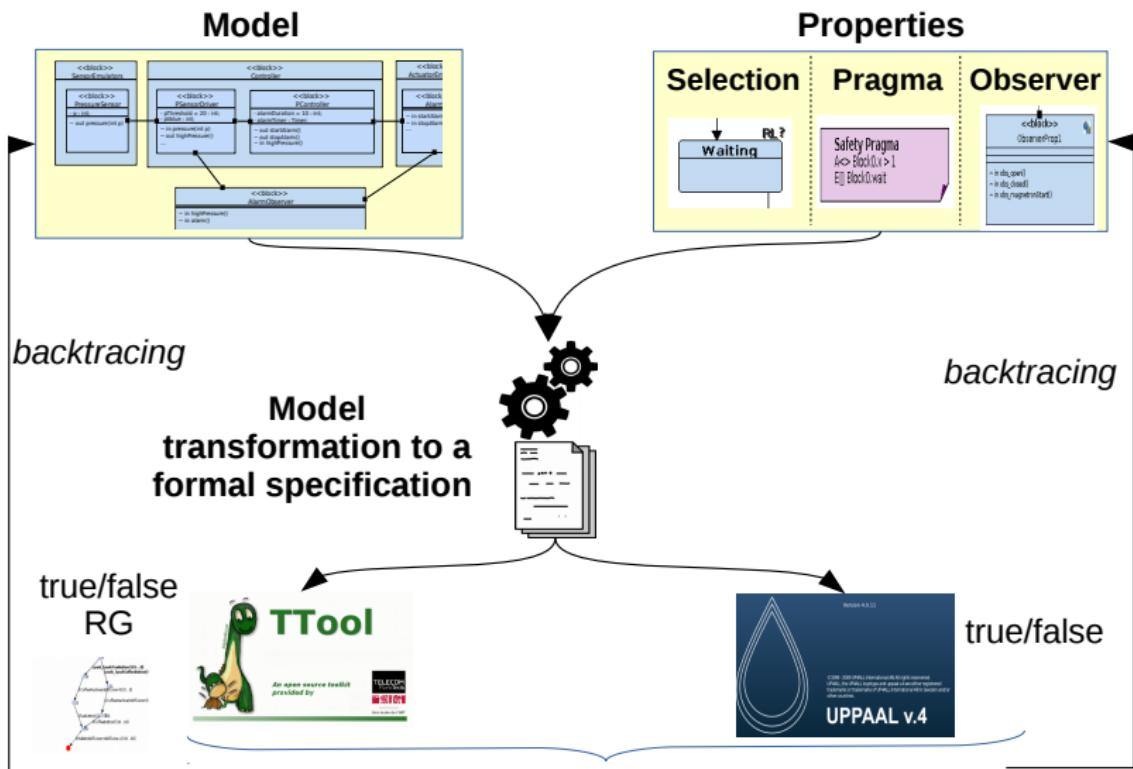
- The experience of the Human who guides the simulation
 - Random selection in case of non deterministic choice (several transitions fireable at the same time)

Formal verification

- Formally checks a model of the system against (a subset of) its expected properties
 - **Formal verification does not rely on chance but on mathematics!**



Safety Verification in TTool



Properties

Example of general properties

- The system shall always reach a given final state
 - From any state the system may return to its initial state
 - Deadlock freeness
 - No unspecified reception (signals are sent but never received)
 - No livelock (systems cannot exit given routines)
 - Never used modeling elements (transitions/states are not reachable)

Properties (Cont.)

Specific properties

E.g. "At any time, one station of the LAN holds the token."

Safety: Nothing bad will happen

E.g. "The microwave oven will not start heating as long as the door remains open."

Liveness: "Something good will eventually happen"

E.g. "All connection requests from a pilot will be acknowledged by an air traffic controller."

Reachability Analysis

Principle of reachability graph generation

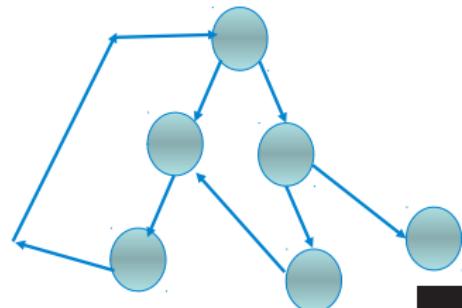
1. From the initial state
 2. Search for fireable transitions and create new states
 3. Compare new states with existing ones
 4. GOTO 2, and take newly created states as initial states

Risk: state explosion problem

- #### ■ Missing resources (e.g. memory)

(Some) Solutions

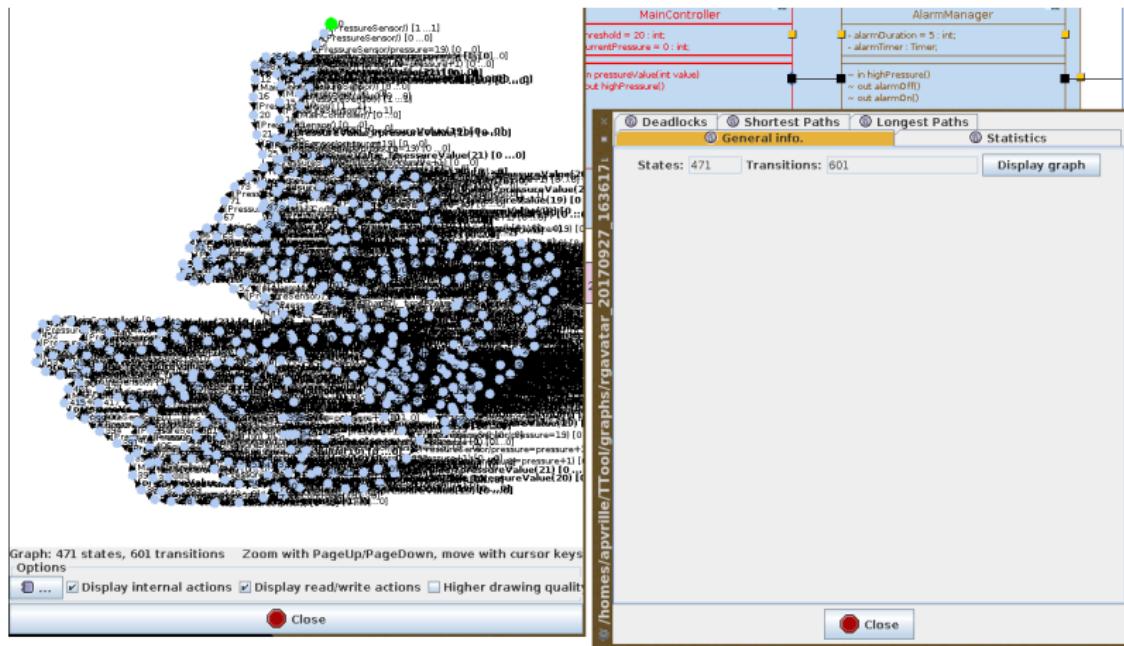
- State coding (hash functions)
 - Partial exploration of the graph



Reachability Graph Generation in TTool

■ Internal feature

- "Syntax checking", then "Avatar Model Checker"



Minimization of Reachability Graph

Graph minimization

Actions ignored

```
!pressureValue_?pressureValue{19} [0 ...]
!pressureValue_?pressureValue{20} [0 ...]
!pressureValue_?pressureValue{21} [0 ...]
!reset_alarmTimer_?reset{} [0 ...0]
!set_alarmTimer_?set{5} [0 ...0]
i(AlarmManager/_timerValue=alarmDura
i(MainController/) [0 ...0]
i(PressureSensor/) [0 ...0]
i(PressureSensor/) [1 ...1]
i(PressureSensor/pressure=19) [0 ...0]
i(PressureSensor/pressure=pressure+1)
```

Actions taken into account

```
!alarmOff_?alarmOff{} [0 ...0]
!alarmOn_?alarmOn{} [0 ...0]
!expire_?expire_alarmTimer{} [0 ...0]
!highPressure_?highPressure{} [0 ...0]
```

<
||
>

Minimization: tools and options

Remove internal actions

Only remove tau transitions

Complete minimization [Experimental]

Select actions and then, click on 'start' to start minimization

Computing list of Actions

1. Cloning graph
2. Making list of actions
3. Sorting actions, and setting graphical lists

All done

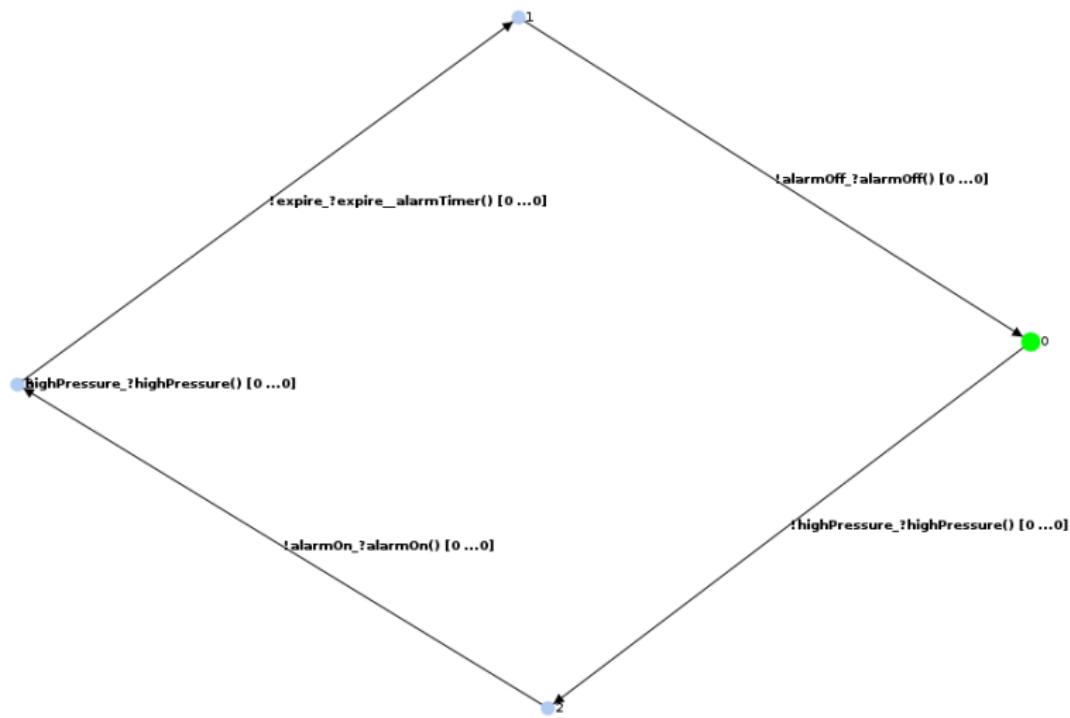
Select actions and then, click on 'start' to start minimization

Minimizing graph...

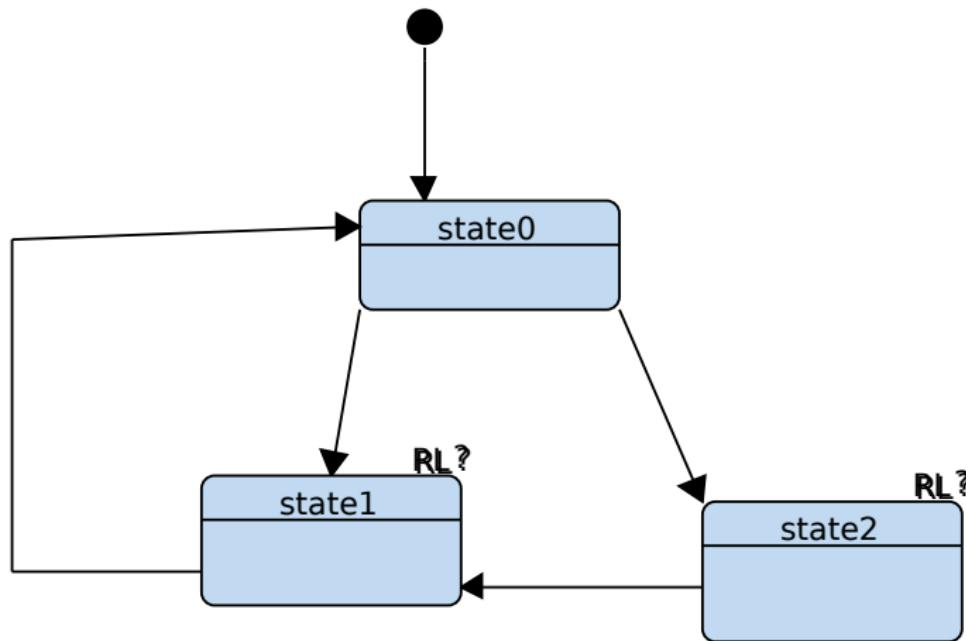
Graph minimized: 4 states, 5 transitions

Start
Stop
Close

Minimized Reachability Graphs

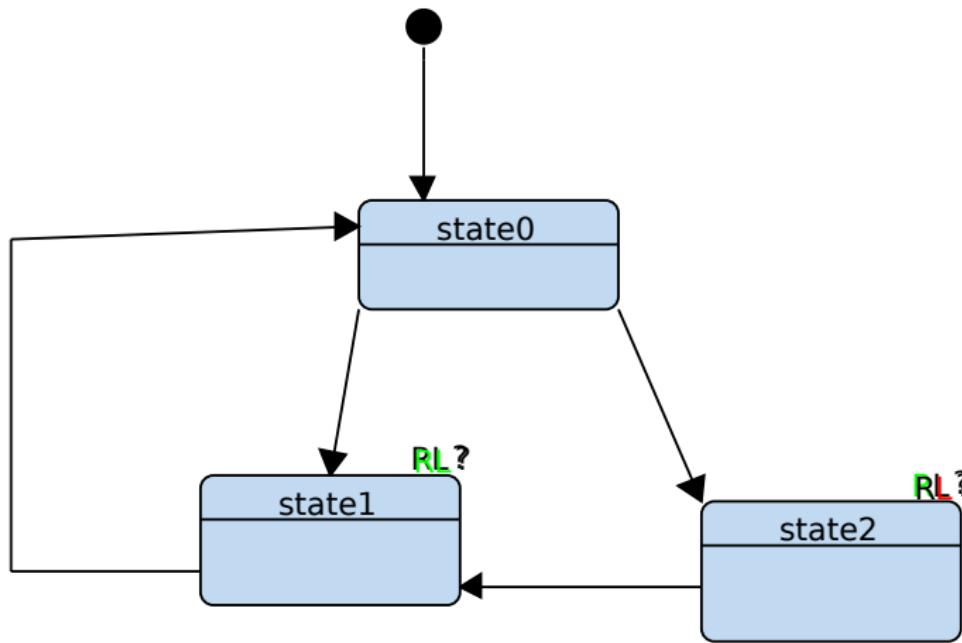


Selecting States for Verification



How to activate "RL" in TTool? Simply right-click on a state and select "Check for Reachability / Liveness"

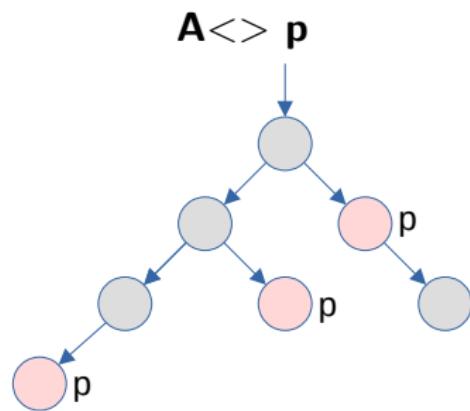
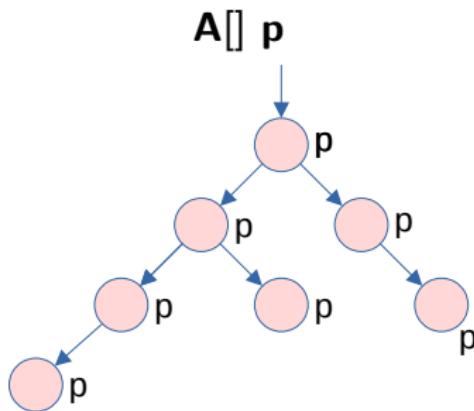
Verification Backtracing



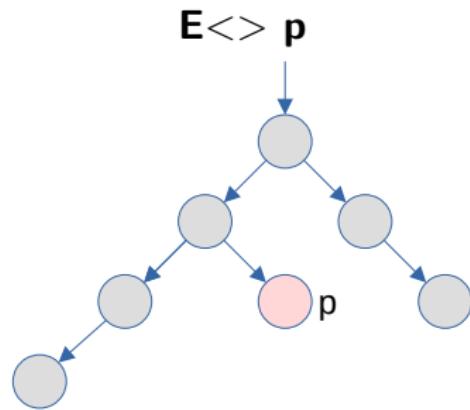
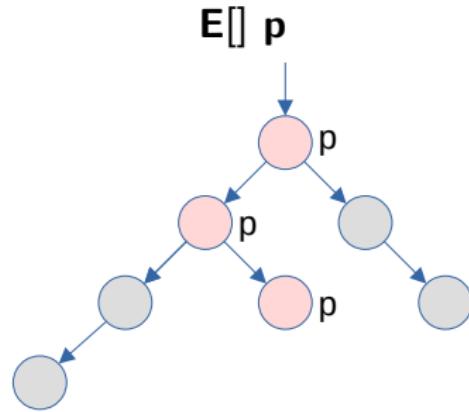
How to obtain this result in TTool? "Syntax checking" then "Safety verification" then check "selected states" in reachability and liveness sections

Safety Pragmas

- TCTL = Timed Computation Tree Logic
 - Two main operators: A (All paths), E (One path)
 - Two modifiers: [] (All states), <> (one state)
 - A (boolean) property p



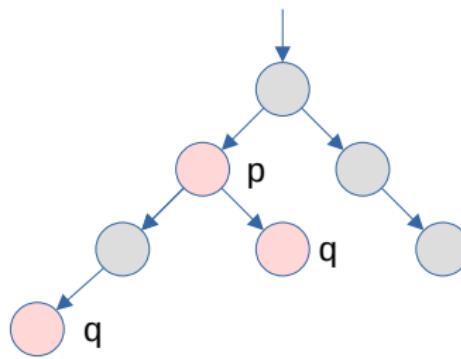
Safety Pragmas (Cont.)



Safety Pragmas (Cont.)

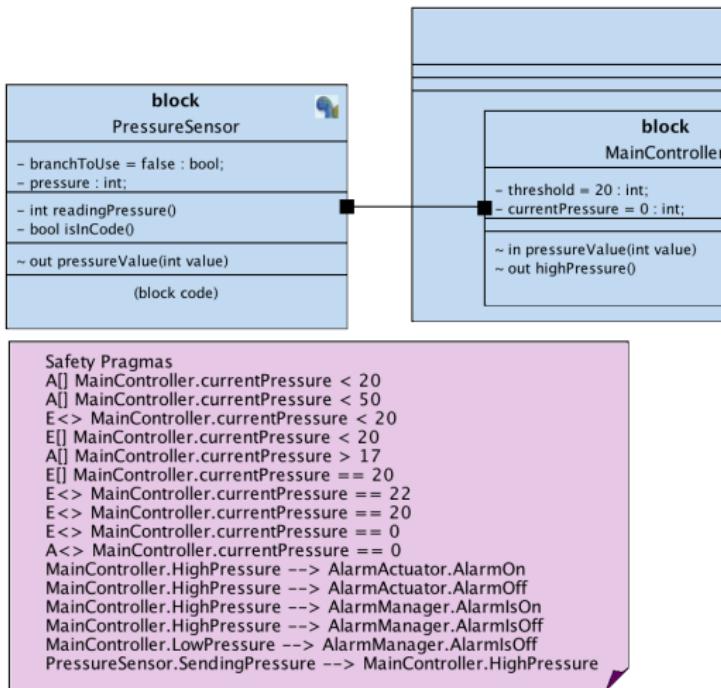
- Leads to
 - $p --> q$

$$p \dashrightarrow q$$



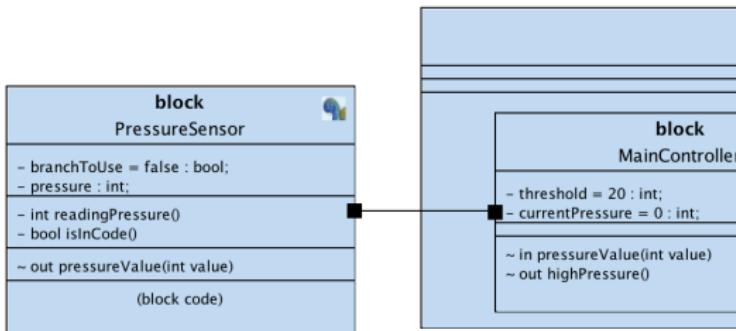
Safety pragmas in TTool

Before verification



Safety pragmas in TTool (Cont.)

After verification



Safety Pragmas

- ✗ A[] MainController.currentPressure < 20
- ✓ A[] MainController.currentPressure < 50
- ✓ E<> MainController.currentPressure < 20
- ✓ E[] MainController.currentPressure < 20
- ✗ A[] MainController.currentPressure > 17
- ✗ E[] MainController.currentPressure == 20
- ✗ E<> MainController.currentPressure == 22
- ✓ E<> MainController.currentPressure == 20
- ✓ E<> MainController.currentPressure == 0
- ✓ A<> MainController.currentPressure == 0
- ✗ MainController.HighPressure --> AlarmActuator.AlarmOn
- ✗ MainController.HighPressure --> AlarmActuator.AlarmOff
- ✓ MainController.HighPressure --> AlarmManager.AlarmsOn
- ✗ MainController.HighPressure --> AlarmManager.AlarmsOff
- ✗ MainController.LowPressure --> AlarmManager.AlarmsOff
- ✗ PressureSensor.SendingPressure --> MainController.HighPressure

Safety pragmas in TTool (Cont.)

- A designer expects a pragma to be true or to be false
- → Expected result can be indicated with a "T" or "F" before the pragma

Safety Pragmas

```

F A[] MainController.currentPressure < 20
T A[] MainController.currentPressure < 50
T E<> MainController.currentPressure < 20
T E[] MainController.currentPressure < 20
F A[] MainController.currentPressure > 17
F E[] MainController.currentPressure == 20
F E<> MainController.currentPressure == 22
T E<> MainController.currentPressure == 20
T E<> MainController.currentPressure == 0
T A<> MainController.currentPressure == 0
F MainController.HighPressure --> AlarmActuator.AlarmOn
F MainController.HighPressure --> AlarmActuator.AlarmOff
T MainController.HighPressure --> AlarmManager.AlarmsOn
F MainController.HighPressure --> AlarmManager.AlarmsOff
F MainController.LowPressure --> AlarmManager.AlarmsOff
F PressureSensor.SendingPressure --> MainController.HighPressure

```



Safety Pragmas

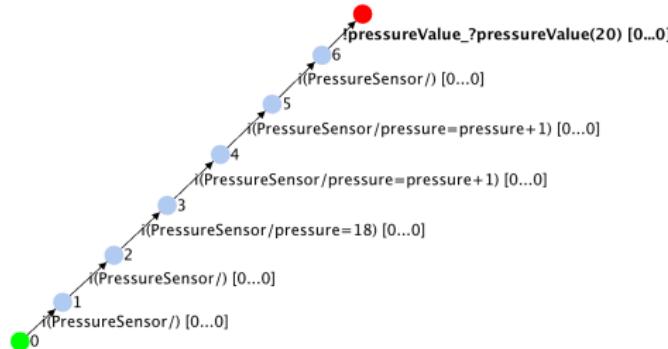
```

✓ F A[] MainController.currentPressure < 20
✓ T A[] MainController.currentPressure < 50
✓ T E<> MainController.currentPressure < 20
✓ T E[] MainController.currentPressure < 20
✓ F A[] MainController.currentPressure > 17
✓ F E[] MainController.currentPressure == 20
✓ F E<> MainController.currentPressure == 22
✓ T E<> MainController.currentPressure == 20
✓ T E<> MainController.currentPressure == 0
✓ T A<> MainController.currentPressure == 0
✓ F MainController.HighPressure --> AlarmActuator.AlarmOn
✓ F MainController.HighPressure --> AlarmActuator.AlarmOff
✓ T MainController.HighPressure --> AlarmManager.AlarmsOn
✓ F MainController.HighPressure --> AlarmManager.AlarmsOff
✓ F MainController.LowPressure --> AlarmManager.AlarmsOff
✓ F PressureSensor.SendingPressure --> MainController.HighPressure

```

Verification Traces

- Traces intend to explain why a pragma is satisfied or not (e.g. proof or counterexample)
- A trace can be displayed as a graph



Trace proving that $A[] \text{MainController.currentPressure} < 20$ is false

Observer-Guided Verification

Observers

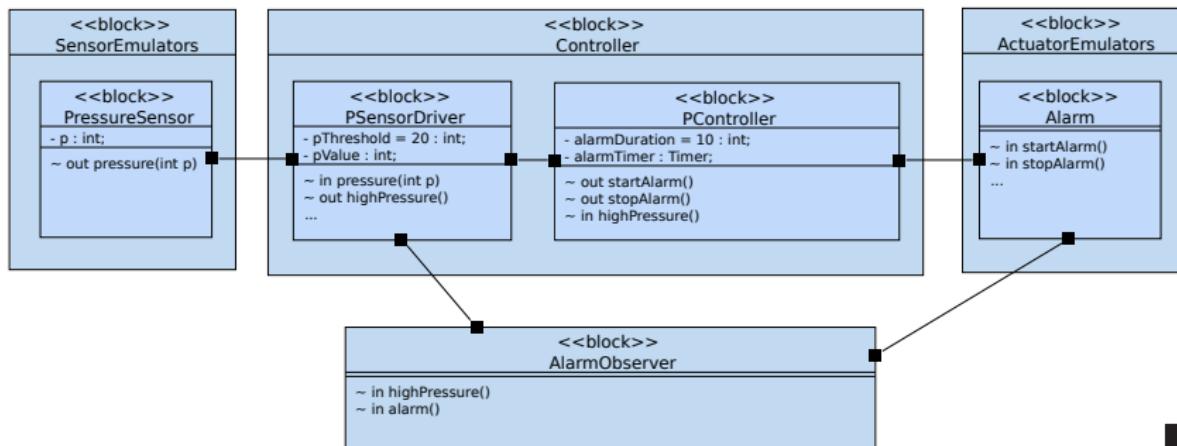
- Expression of (complex) properties within the design
- Observer should have an *error* state whose reachability can be searched for in TTool/UPPAAL
- The observer should remain non-intrusive
 - At least, as long as the observed property is satisfied

Example: Pressure Controller

- Observer that verifies the alarm rings in zero time when a high pressure is detected

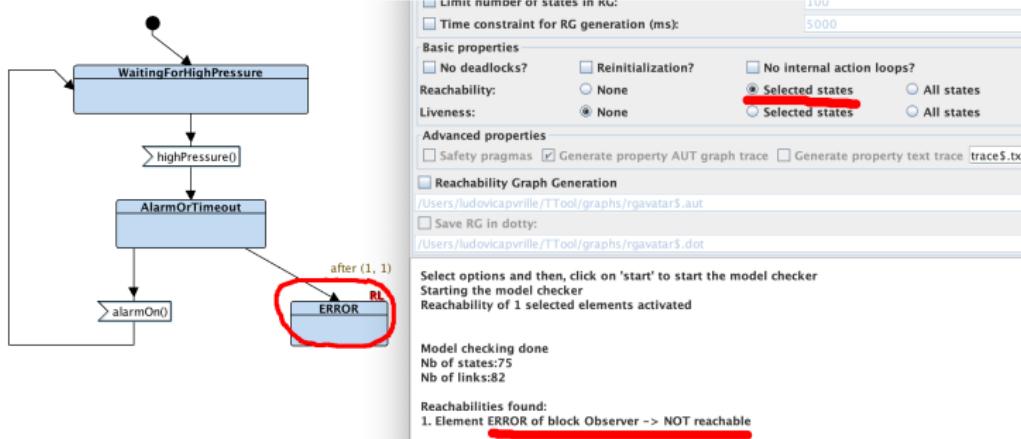
Pressure Controller: Design of an Alarm Observer

- An "AlarmObserver" block is added to the design
- AlarmObserver fetches information from the pressure sensor and the alarm



Pressure Controller: Design of an Alarm Observer (Cont.)

- Whenever the observer gets a *highPressure* signal, it goes into the state ERROR after 1 unit of time if it hasn't received yet an *alarm* signal
- The reachability of ERROR is searched for



Outline

Model Simulation

Formal verification

Rapid prototyping and code generation

Code generation

Virtual prototyping

Customizing code generation in TTool

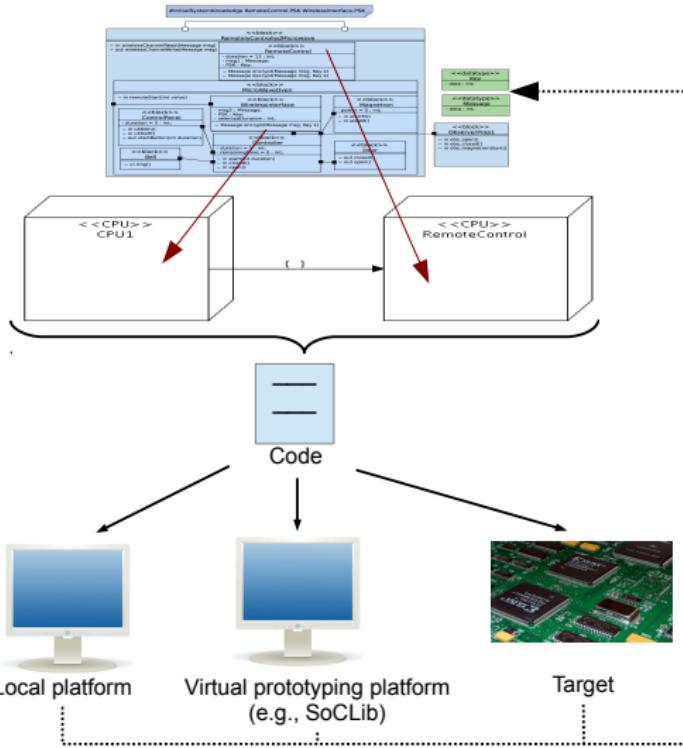
Introduction to Rapid Prototyping

Rapid prototyping intends to experiment with the execution of code produced from models

Content

- Overview of code generation in TTool
 - Transformation of AVATAR design diagrams into executable code
 - Application to a microwave oven

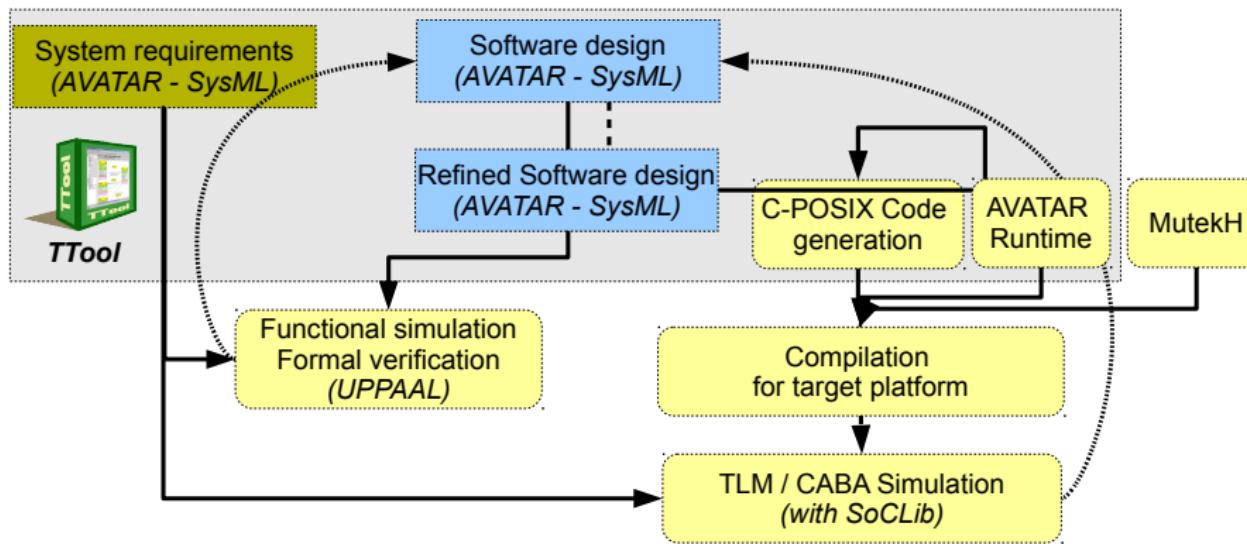
Code Generation: Overview



Principle of Code Generation

- Only AVATAR design diagrams are taken into account
 - Generated code relies on POSIX threads
 - One thread per block
 - Synchronous communications between blocks is implemented in the AVATAR runtime with POSIX mutex
 - Asynchronous communications relies on linked lists managed in the AVATAR runtime
 - Time is handled based on POSIX *clock_gettime()* with *CLOCK_REALTIME* option
 - ...

Virtual Prototyping: Method



Virtual Prototyping Steps

1. Model refinement
 2. Selection of an OS, setting of options of this OS (scheduling algorithm, ...)
 3. Selection of a hardware platform, and selection of a task allocation scheme
 4. Code generation (press-button approach)
 5. Manual code improvement - Code might also be manually added at model level
 6. Code compilation and linkage with OS
 7. Simulation platform boots the OS and executes the code
 8. Execution analysis: directly in TTool (sequence diagram), with debuggers (e.g., *gdb*), or with custom graphical interfaces

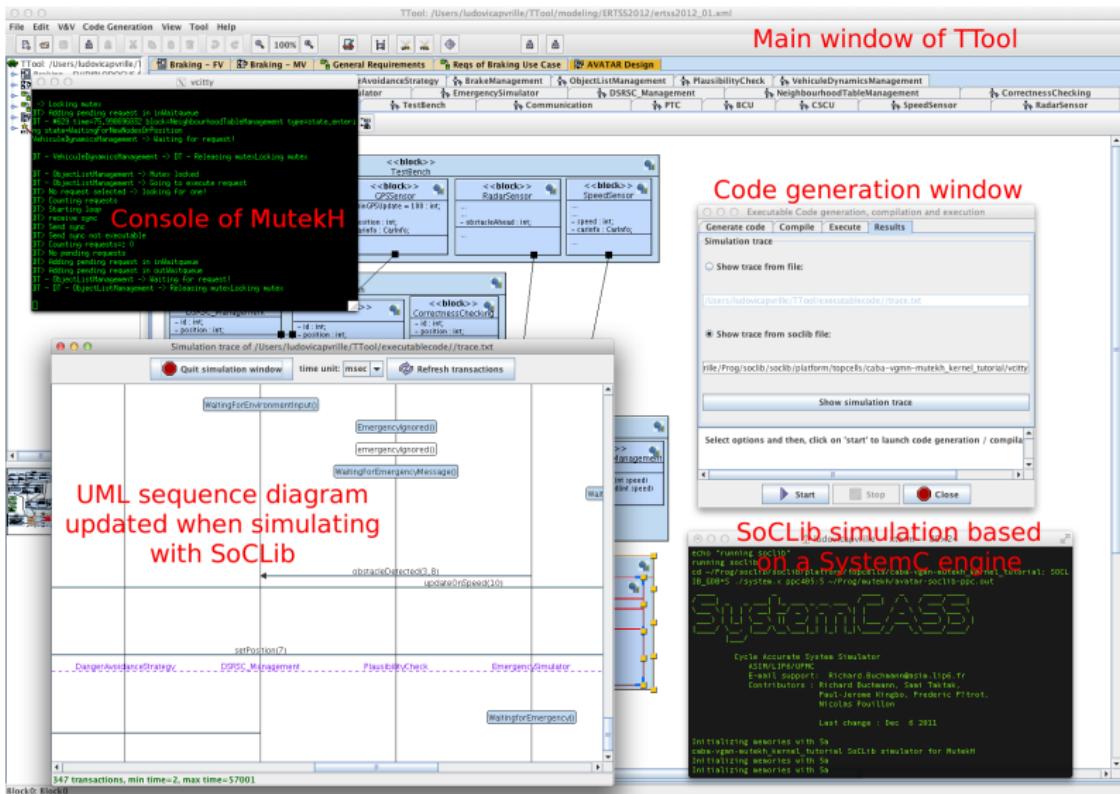
Support: SoCLib and MutekH

Hardware platform simulator: SoCLib (www.soclib.fr)

- Virtual prototyping of complex Systems-on-Chip
 - Supports several models of processors, buses, memories
 - Example of CPUs: MIPS, ARM, SPARC, Nios2, PowerPC
 - Two sets of simulation models:
 - TLM = Transaction Level Modeling
 - CABA = Cycle Accurate Bit Accurate

- Natively handles heterogeneous multiprocessor platforms
 - POSIX threads support
 - Note: any Operating System supporting POSIX threading and that can be compiled for SoCLib could be used

Virtual Prototyping: Graphical Environment



TELECOM
Paris

(Virtual) Prototyping: Code Generation

The screenshot shows a software application window titled "Executable Code generation, compilation and execution". The window has a toolbar at the top with four tabs: "Generate code" (selected), "Compile", "Execute", and "Results". Below the toolbar, the "Code generation" section is active. It contains a "Base directory of code generation code:" field set to "/Users/ludovicapvrille/TTool/executablecode/", and several configuration checkboxes:

- Remove .c / .h files
- Remove .x files
- Put debug information in generated code
- Put tracing capabilities in generated code
- Optimize code

A "1 time unit =" label followed by a dropdown menu set to "sec". The "Code generator used:" dropdown menu is set to "AVATAR CPOSIX". A large text area at the bottom prompts the user to "Select options and then, click on 'start' to launch code generation / compilation / execution". At the bottom of the window are three buttons: "Start" (blue background), "Stop" (gray background), and "Close" (red octagon background).

Virtual Prototyping: SocLib Simulation

echo "running soclib"
running soclib
cd ~/Prog/soclib/soclib/platiorr/topcelis/caba-vgmn-mutekh_kernel_tutorial; SOCLIB_GDB=5 ./system.x ppc405:5 ~/Prog/mutekh/avatar-soclib-ppc.out

SOCLIB

Cycle Accurate System Simulator
ASIM/LIP6/UPMC
E-mail support : Richard.Buchmann@asim.lip6.fr
Contributors : Richard Buchmann, Sami Taktak,
Paul-Jerome Kingbo, Frederic P?trot,
Nicolas Pouillon

Last change : Dec 6 2011

Initializing memories with 5a
cabal-vgmn-mutekh_kernel_tutorial SoClib simulator for Mutekh
Initializing memories with 5a
Initializing memories with 5a

Virtual Prototyping: Console

```
vcitty

-> Locking mutex
DT> Adding pending request in inWaitqueue
DT - #629 time=75.998696832 block=NeighbourhoodTableManagement type=state_entering state=WaitingForNewNodesOrPosition
VehiculeDynamicsManagement -> Waiting for request!

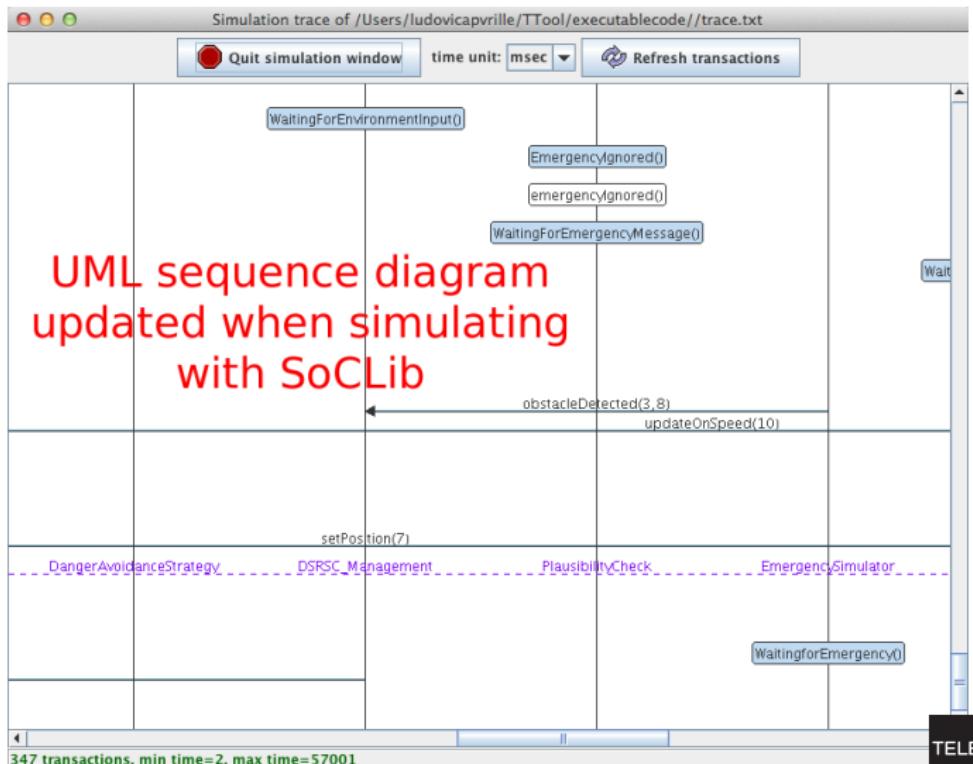
DT - VehiculeDynamicsManagement -> DT - Releasing mutexLocking mutex

DT - ObjectListManagement -> Mutex locked
DT - ObjectListManagement -> Going to execute request
DT> No request selected -> looking for one!
DT> Counting requests
DT> Starting loop
DT> receive sync
DT> Send sync
DT> Send sync not executable
DT> Counting requests:= 0
DT> No pending requests
DT> Adding pending request in inWaitqueue
DT> Adding pending request in outWaitqueue
DT - ObjectListManagement -> Waiting for request!
DT - DT - ObjectListManagement -> Releasing mutexLocking mutex
```

Console of MutekH

(Virtual) Prototyping: Trace

TTool displays execution traces in a sequence diagram



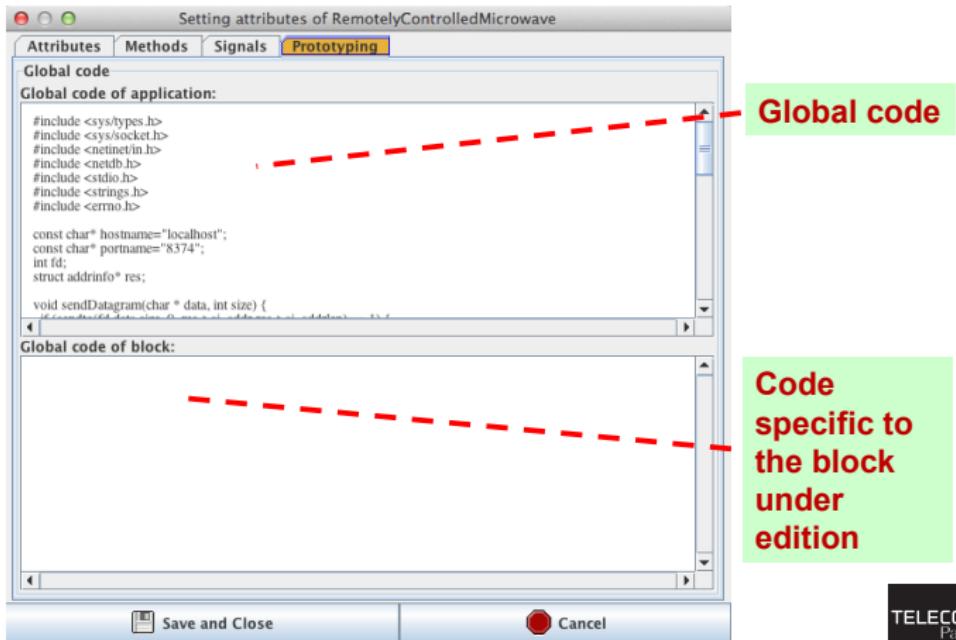
Customizing Generated Code with Your Own Code: Application and Block Code

- Global code of the application

- Inclusion of header files, global variables,

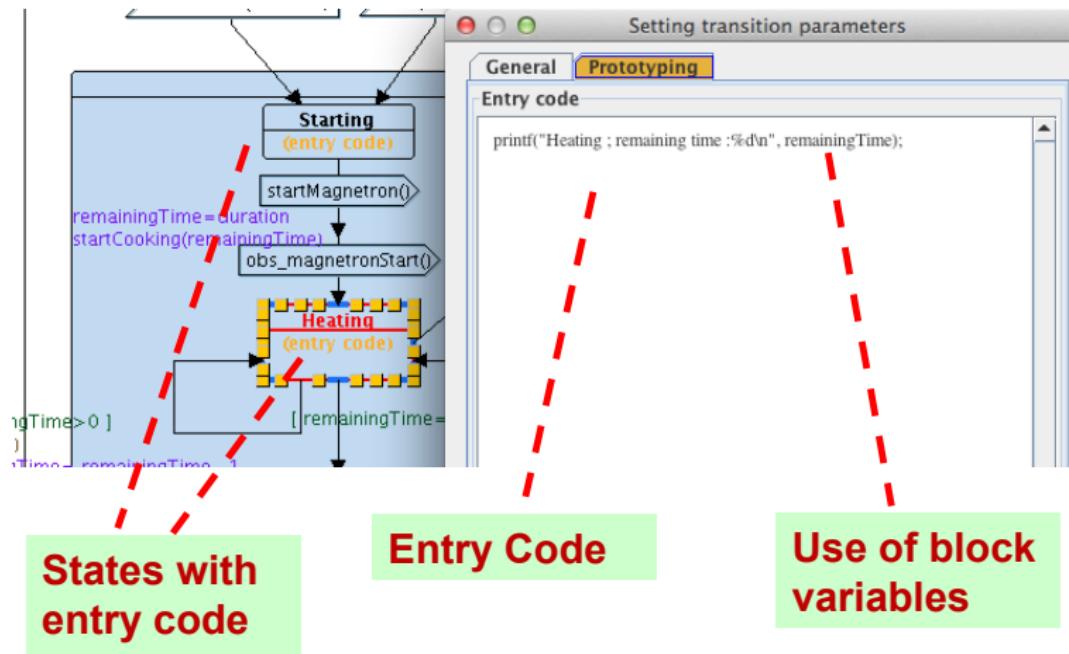
• • •

- Code global to one given block



Customizing Generated Code with Your Own Code: State Entry Code

- Code executed whenever a state is reached



Use of Customized Generated Code

Console debug

- Using e.g. *printf()* function

Connection to a graphical interface

- Piloting the code with a graphical interface
 - Visualizing what's happening in the executed code
 - Connection to graphical interface via, e.g., *sockets*

Use of Customized Generated Code (Cont)

Graphical interface for the microwave oven

- Socket connection to a graphical interface programmed in Java

